

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. / 10559-607001 ✓	Application No. / 10/054,179 ✓
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant William R. Wheeler et al. ✓	
		Filing Date January 17, 2002 ✓	Group Art Unit 2123 / 2825 ✓

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
[Handwritten Initials]	AA	2002/0049957	04/2002	Hosono et al.			
	AB	6,233,723	05/2001	Pribetich			
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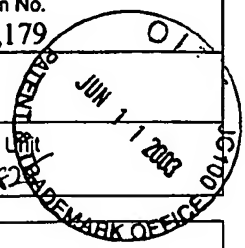
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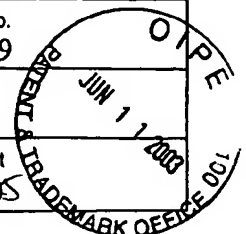


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	AEE	6,272,671	08/2001	Fakhry			
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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ACCC						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	ADDD							
	AEEE							
	AFFF							

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	AHHH	Pedram et al., "Floorplanning with Pin assignment", 1990 IEEE International Conference on Computer-Aided Design, 11 November 1990, pp. 98-101.
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	AJJJ	Mentor Graphics Corporation, Renoir™ With HDL2Graphics™, pp. 1-6, 1998, Oregon.
	AKKK	Mentor Graphics Corporation, Renoir HDL Design Datasheet, pp. 1-2, 1999, Oregon.
	ALLL	Computer Design, "AFTER HARD KNOCKS, CYCLE-BASED SIMULATORS STAND THEIR GROUND". http://www.computer-design.com/Editorial/1996/10/ASIC/after.html , accessed on August 23, 2001, pages 1-5.
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	ANNN	
	AOOO	

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	AFF	5,974,242	10/1999	Damarla, et al.			
	AGG	6,077,304	06/2000	Kasuya			
	AHH	6,161,211	12/2000	Southgate			
	AII	6,178,541	01/2001	Joly, et al.			
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	AVV	6,421,816	07/2002	Ishikura			
	AWW	6,438,729	08/2002	Ho			
	AXX	6,438,731	08/2002	Segal			
	AYY	6,440,780	08/2002	Kimura, et al.			
	AZZ	6,473,885	10/2002	Wallace			
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(37 CFR 1.98(b))

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	AJJJ	6,591,407	07/2003	Kaufman, et al.			
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	ALLL	2002/0059054	05/2002	Bade, et al.			
	AMMM	2002/0112221	08/2002	Ferreri, et al.			
	ANNN	2002/0138244	09/2002	Meyer			
	AOOO	2003/0004699	01/2003	Choi, et al.			
	APPP	2003/0036871	02/2003	Fuller, et al.			
	AQQQ	2003/0177455	09/2003	Kaufman, et al.			

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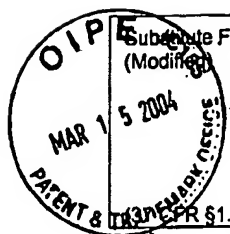
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	ARRR	0 404 482	12/1990	EPO				
	ASSS	0 433 066	06/1991	EPO				
	ATTT	0 720 233	07/1996	EPO				
	AUUU	0 901 088	03/1999	EPO				
	AVVV	1 065 611	01/2001	EPO				
	AWWW	58-060559	04/1983	Japan				
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	AYYY	07-049890	02/1995	Japan				
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Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
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	AHHHH	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
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	AJJJJ	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", <i>Electrical Design News</i> , 41(14):129-136 (1996).
	AKKKK	NB84035598, "Binary Relational Schema to Model Structured LSI Design", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pp. 5598-5601.
	ALLLL	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.
	AMMMM	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
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	AOOOO	Parlakbilek, et al., "A Multiple-Strength Multiple-Delay Compiled-Code Logic Simulator", <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 12(12):1937-1946 (1993).
	APPPP	Su, Stephen, "An Interactive Design Automation System", <i>Proceedings of the 10th Design Automation Workshop on Design Automation</i> , pp. 253-261, June 1973.
	AQQQQ	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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